SSC8313GS1

Dual P-Channel Enhancement Mode MOSFET

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
-16V	±8V	35mΩ@-4V5	-9A
		56mΩ@-2V5	

➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. Excellent thermal and electrical capabilities.

100% UIS + ΔVDS + Rg Tested!

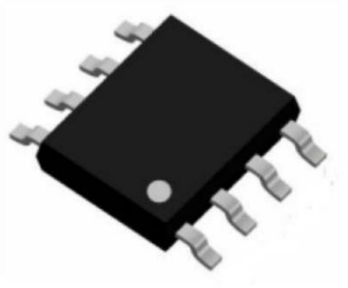
➢ Applications

- NB Battery
- DC/DC Conversion
- Load Switch

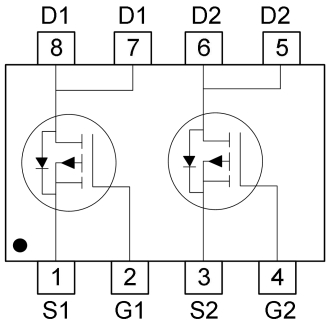
➢ Ordering Information

Device	Package	Shipping
SSC8313GS1	SOP-8	4000/Reel

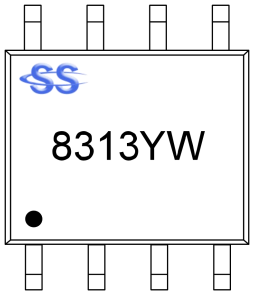
➢ Pin configuration



SOP-8



Pin Configuration (Top View)



Marking

(YW: Internal Traceability Code)

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-to-Source Voltage		-16	V
V_{GSS}	Gate-to-Source Voltage		±8	V
I_D	Continuous Drain Current [d]	T_C=25℃	-9.0	A
		T_C=100℃	-5	
I_{DSM}	Continuous Drain Current [a]	T_A=25℃	-5.8	A
		T_A=70℃	-4.3	
I_{DM}	Pulsed Drain Current [b]		-36	A
P_D	Power Dissipation [c]	T_C=25℃	5	W
		T_C=100℃	2	
P_{DSM}	Power Dissipation [a]	T_A=25℃	2.1	W
		T_A=70℃	1.33	
E_{AS}	Avalanche Energy [b] L=0.5mH Single Pulse		46	mJ
T_J	Operation junction temperature		-55~150	℃
T_{STG}	Storage temperature range		-55~150	

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	60	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	25	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

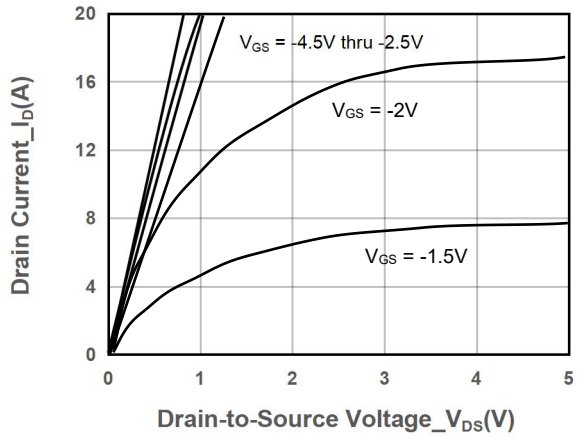
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

d. The value of $R_{\theta JC}$ has been determined of the temperature difference between junction and the case surface in contact with water cooled copper heat sink.

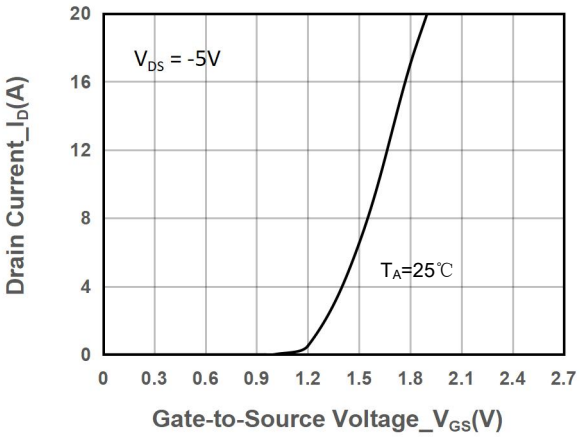
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250uA	-16			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-0.45	-0.75	-1.2	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -3.5A		35	60	mΩ
		V_{GS} = -2.5V, I_D = -3A		56	90	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	uA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -1.6A	-0.5	-0.75	-1.2	V
Gate Resistance	R_G	V_{DS} = 0V, f = 1MHz		1.8		Ω
Input Capacitance	C_{ISS}	V_{DS} = -8V, V_{GS} = 0V, f = 1MHz		1262		pF
Output Capacitance	C_{OSS}			161		
Reverse Transfer Capacitance	C_{RSS}			138		
Total Gate charge	Q_g	V_{GS}=-4.5V, V_{DS}=-8V, I_D=-3A		20		nC
Gate to Source charge	Q_{gs}			4.1		
Gate to Drain charge	Q_{gd}			4.3		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = -4.5V, V_{DS} = -8V, R_L = 2Ω, R_G = 6Ω, I_D =-3A		25		ns
Rise time	T_r			30		
Turn-off Delay Time	$T_{D(OFF)}$			42		
Fall time	T_f			28		

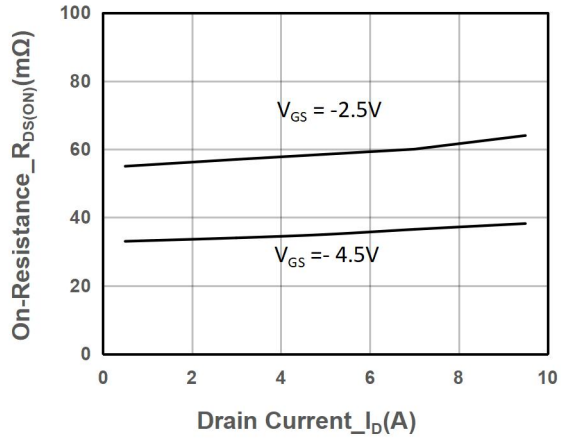
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



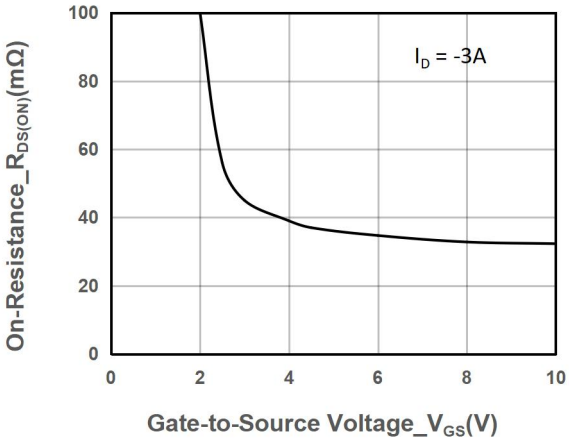
Output Characteristics



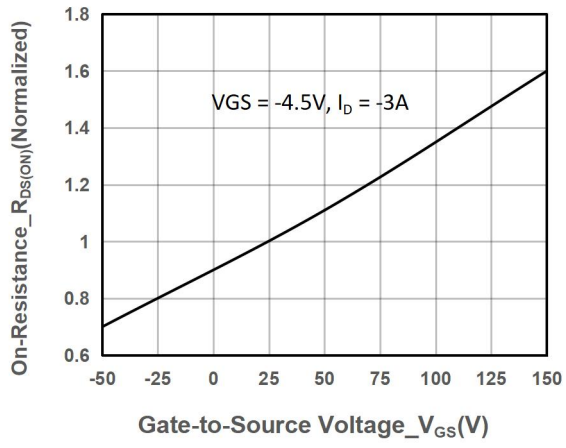
Transfer Characteristics



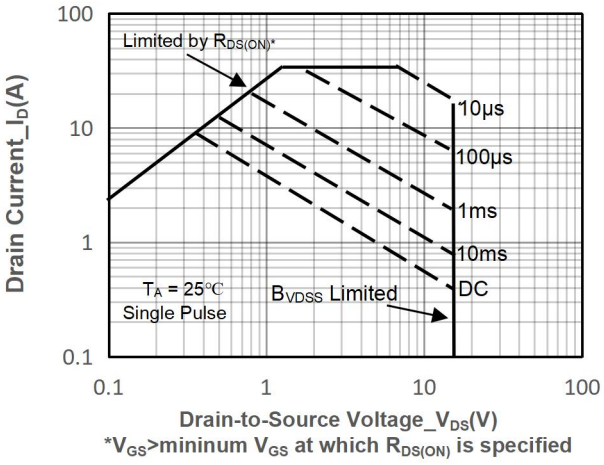
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

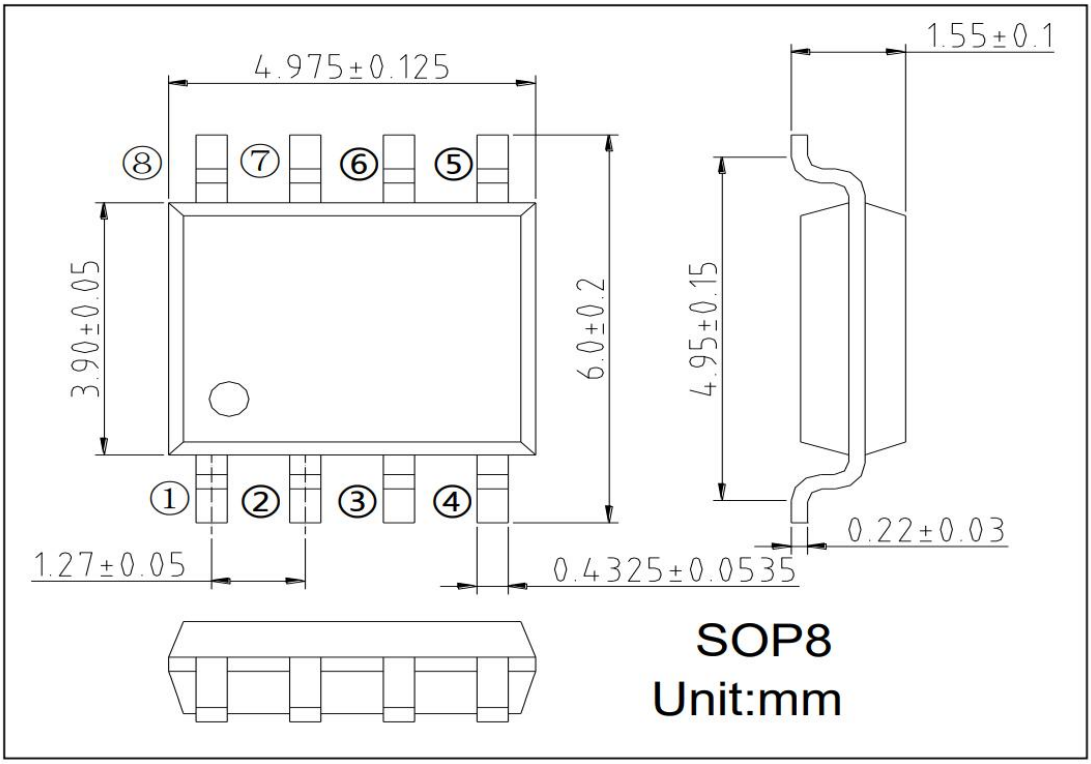


On-Resistance vs. Junction Temperature



Safe Operating Area vs. Junction-to-Ambient

➢ Package Information



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